RTC6715 CMOS 5.8GHz Band FM Receiver

Product Description

The RTC6715 is a highly integrated FM receiver intended for application on 5.8GHz band FM demodulation. This chip includes a low noise amplifier, mixer, IF amplifier, FM demodulator, AGC, audio demodulators, audio Amps and noise squelch. With RSSI voltage output, the instantaneous radio signal strength can be monitoring. RTC6715 is able to demodulate the FM modulated video and Stereo audio signals sourced from RTC6705 and separate the desired signal at the dedicated output pins. Both Stereo and Mono application are available on the chip.

RTC6715's operation frequency can be set by SPI programming, or by selecting six dedicated pins. Both CE and FCC regulations are easy to pass by using RTC6715 with application circuit and single room shielding case.

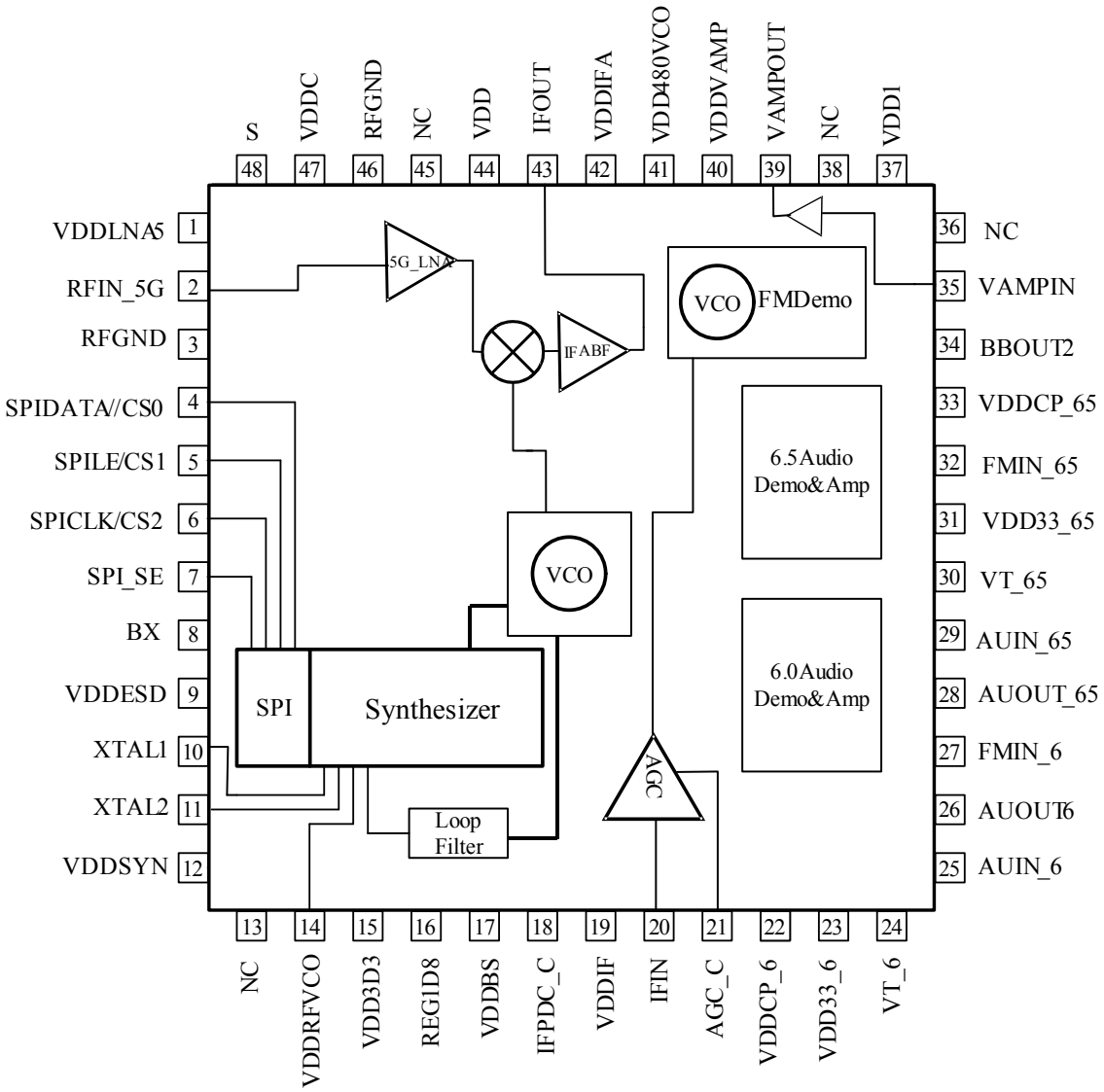
Features

- Single 3.3V supply power
- 5.8GHz band FM demodulator with two audio subcarrier demodulators at 6MHz/6.5MHz
- High sensitivity -85dBm
- Simple six digital pins setting 24 fixed channels to eliminate external micro-controller
- Radio Strength Indicator (RSSI)
- Hard mute by noise squelch
- CMOS technology Single chip with integrated VCO and PLL
- 48-pin Leadless QFN package pass RoHS

Application

- AV Sender
- Surveillance
- Baby Monitor
- Wireless Camera
- Wireless Audio
- Wireless Earphone

Block Diagram



Pin Descriptions

PIN	NAME	I/O	FUNCTION
1	VDDLNA5	Supply In	3.3V for RX LNA5G
2	RFIN_5G	Analog In	5 GHz LNA input for RF input signal
3	RFGND	Analog GND	RF ground
4	CS0	Digital In	Easy channel selection (Internal pull high) [1]
	SPIDATA	Digital In	SPI bus data input[1]
5	CS1	Digital In	Easy channel selection (Internal pull high) [1]
	SPILE	Digital In	SPI bus latch enable input[1]
6	CS2	Digital In	Easy channel selection (Internal pull high) [1]
	SPICLK	Digital In	SPI bus clock input[1]
7	SPI_SE	Digital In	Switch mode or SPI selection [1]
8	BX	Digital In	At easy channel selection mode : BX is used for alternative band selection [1] At SPI mode : BX is Don't care
9	VDDESD	Supply In	3.3V
10	XTAL1	Analog In	Crystal Input
11	XTAL2	Analog In	Crystal Input
12	VDDSYN	Digital Ground	3.3V for RF synthesizer
13	NC		Not connected
14	VDDRFVCO	Supply In	3.3V for 5GHz VCO
15	VDD3D3	Supply In	3.3V for digital 1.8V regulator
16	REG1D8	Analog Out	Regulator 1.8V for Digital block
17	VDDBS	Supply In	3.3V for Bias
18	IFPDC_C	Analog Out	RSSI Out
19	VDDIF	Supply In	3.3V for IFAAF
20	IFIN	Analog In	IFA_AF inputs
21	AGC_C	Analog I/O	AGC Rectifier output
22	VDDCP_6	Supply In	3.3V for 6MHz charge pump and VCO
23	VDD33_6	Supply In	3.3V for 6MHz audio amplifier
24	VT_6	Analog Out	Audio demo out for 6MHz VCO
25	AUIN_6	Analog IN	Audio amplifier in for 6MHz path
26	AUOUT6	Analog Out	Audio amplifier out for 6MHz path
27	FMIN_6	Analog In	6MHz FM audio in
28	AUOUT_65	Analog Out	Audio amplifier out for 6.5MHz path
29	AUIN_65	Analog In	Audio amplifier in for 6.5MHz path
30	VT_65	Analog Out	Audio demo out for 6.5MHz VCO
31	VDD33_65	Supply In	3.3V for 6.5MHz audio amplifier
32	FMIN_65	Analog In	6.5MHz FM audio in
33	VDDCP_65	Digital In	3.3V for 6.5MHz charge pump and VCO
34	BBOUT2	Analog Out	FMDeMod Buffer output
35	VAMPIN	Analog In	Video amp input
36	NC		Not connected
37	VDD1	Supply In	3.3V
38	NC		Not connected
39	VAMPOUT	Analog Out	Video amp output
40	VDDVAMP	Supply In	3.3V for Video Amp
41	VDD480VCO	Supply In	3.3V for FM demod VCO

Pin Descriptions (continued)

PIN	NAME	I/O	FUNCTION
42	VDDIFA	Supply In	3.3V for RX IFAs
43	IFOUT	Analog Out	IF OUT
44	VDD	Supply In	3.3V VDD
45	NC		Not connected
46	RFGND	Analog GND	RF ground
47	NC		Not connected
48	S	Digital In	A/B band selection [1] 0 for A band; 1 for B band

Note 1. Digital pins, BX, SPI_SE and SPIDATA/CS0, SPILE/CS1 and SPICLK/CS2 are internal pull-high circuits.

Electrical Specification

(1) Absolute Maximum Ratings

SYMBOL	PARAMETER	Ratings	UNIT
Tstr	Storage Temperature Range	-65 to +150	°C
Totr	Operating Temperature Range	-40 to +85	°C
Vdd	Supply Voltage	-0.5 to +5	V
Vlog	Logic control signal	-0.5 to +5	V
VRX	RX input	-2 to +2	V

The maximum rating must not be exceeded at any time. Do not operate the device under conditions outside the above

(2) DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Tj	Temperature Range		-40	25	85	°C
VDD33	3.3V Supply Voltage		3.1	3.3	3.5	V
I_module	Power consumption under test circuit and color-bar test pattern	TT 25C, 3.3V		195		mA
Icc	Power consumption	TT 25C, 3.3V		146		mA
Fref	Oscillator operating frequency			8		MHz
V_IH	High Level Input Voltage for Digital Interface	V_IO=3V	0.7xV_IO		V_IO+0.3	V
V_IL	Low Level Input Voltage for Digital Interface		-0.3		0.3xV_IO	V

(3) 5GHz Band FM Receiver Specifications (VDD=+3.3V, 25℃)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
RF_Freq	RF Input frequency		5725		5865	MHz
IF_Freq	IF output frequency		479	480		MHz
S11	RF Input return loss under test circuit	External matching@50Ω		-10		dB
Si	Input Sensitivity measurement under test circuit	SNR 43dB Fmod=15KHz Frequency deviation :±2.5MHz LPF BW:20KHz		-85		dBm
Phase noise	LO: 5246MHz	100KHz offset 1MHz offset		-90 -112		dBc/Hz
VRSSI	RSSI output voltage	-91dBm 5dBm		0.5~1.1		V
Z22_IFout	IF 480MHz output Impedance	SE		50		Ω
Z22_IFin	IF 480MHz Input Impedance	SE		50		Ω
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Video						
V_pp	Vpp after video clamping	75ohm load		1		Vpp
Audio						
Carrier_Freq	Audio carrier frequency			6/6.5		MHz
Output signal level	Vpp after Audio Amplifier	Fmod: 1KHz tone Frequency deviation: ±25Khz Load: > 1Kohm		1		Vpp
Max_App	Maxmum Vpp after Audio amplifier with distortion <1%	Fmod: 1KHz tone Frequency deviation: ±50Khz Load: > 1Kohm		2		Vpp
THD	Total harmonic distortion Output 1Vpp (1KHz tone)	Fmod: 1KHz tone Frequency deviation: ±25Khz Load: > 1Kohm		1%		%
S/N	Audio SNR (as reference design,) With pre-emphasis/ de-emphasis	Fmod: 1KHz tone with 2Vpp audio output Load: > 1Kohm		56		dB

(4) SPI Digital Timing Diagram

In SPI Mode (**SPI_SE = 1**), the 3-wire SPI interface is used to configure the frequency as well as internal registers. Series data sequence of 3-wire SPI is shown in following Figure. This **25-bit** data stream consists of **4 address bits**, 1 read/write control bit and 20 data bits. Data transfer is LSB first.

During write cycle (R/W = 1), the chip will sample the **SPIDATA** on the rising edge of **SPICLK**. Sampled data will be temporally stored in internal shift register. One the rising edge of **SPILE**, data in shift register will be latched into specific register according to the address.

During read cycle (R/W = 0), address and read/write control bit are sampled at rising edge of **SPICLK**, but the data bits are sent at the falling edge of **SPICLK**.

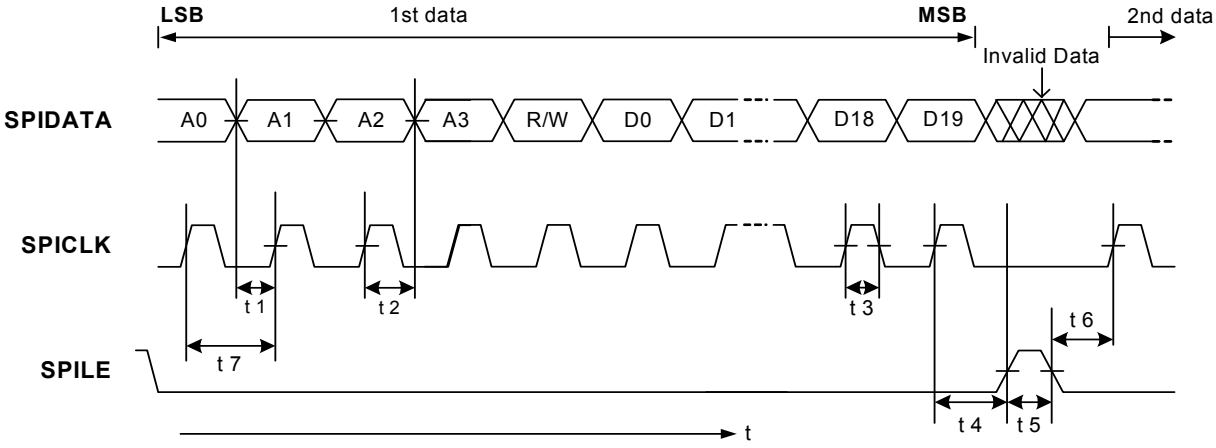


Figure 6.1 Series data sequence on SPI interface of RTC6716

Parameter	Min.	Typ.	Max.	Unit
t1	20	-	-	ns
t2	20	-	-	ns
t3	30	-	-	ns
t4	30	-	-	ns
t5	100	-	-	ns
t6	20	-	-	ns
t7	100	-	-	ns

Note:
1.) On the rising edge of the SPICLK, one bit of data is transferred into the shift register.
2.) SPILE should be “L” when the data is transferred into the shift register.

Channel Selection Table

When pin 7 (SPI_SE) is set at low voltage, the chip works as in the easy channel selection mode and the pins 4(SPIDATA/CS0), 5(SPILE/CS1), 6(SPICLK/CS2)，48(S) and 8(BX) are used for channel selection. Channel frequencies refer to below table.

	SPI_SE	Band	BX	S	CS[2:0]							
					000	001	010	011	100	101	110	111
5GHz Band	0	A	0	0	5865M	5845M	5825M	5805M	5785M	5765M	5745M	5725M
	0	B	0	1	5733M	5752M	5771M	5790M	5809M	5828M	5847M	5866M
	0	E	1	X	5705M	5685M	5665M	5645M	5885M	5905M	5925M	5945M
	1	SPI	X	X	three wire SPI control pins							

SPI mode

When pin 7 (SPI_SE) is set at high (3.3V), the chip works as in the SPI mode and the pins 4(SPIDATA/CS0), 5(SPILE/CS1) and 6(SPICLK/CS2) are used for 'SPI' inputs for 3-wire programming

Address 0x00: Synthesizer Register A

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–					SYN_RF_R_REG [14:0]														
5G Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

SYN_RF_R_REG [14:0]:	**Default** **5.8GHz: 0010H** R-counter divider ratio control for RF Synthesizer. For 5.8GHz Default: 0**0008H** Crystal clock (F_{osc})=: 8MHz Reference clock=crystal clock/R-counter=8MHz/8=1MHz

Address 0x01: Synthesizer Register B

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYN_RF_N_REG [12:0]													SYN_RF_A_REG [6:0]						
5G Default	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0	1

Default **5.8GHz: 02A05H** Synthesizer counter default setting (5.8Ghz band:5865MHz) For 5.8Ghz band, **F_{LO} = 2*(N*32+A)*(F_{osc}/R)** Example: default F_{RF}=5865MHz, F_{LO}=5865-479=5386MHz, F_{osc}=8MHz, R=8 5385/2=(N*32+A)*8Mhz/8=2*(N*32+A)*1MHz N=84(=1010100), A5(=0101) For 5.8GHz default: **02A05H**	
SYN_RF_N_REG [12:0]:	N counter divider ratio control for RF Synthesizer.
SYN_RF_A_REG [6:0]:	A counter divider ratio control for RF Synthesizer.

Address 0x02: Synthesizer Register C

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGC_6M [2:0]			AGC_6M5 [2:0]			CC_VCO [1:0]		CP_5GLO [2:0]			CP_FT [2:0]			SC_CTL	MOUT [1:0]		PRES_FT [2:0]		
Default	1	1	0	1	1	0	1	1	0	1	1	0	0	1	0	0	0	0	1	1

Default: FFE44H	
AGC_6M [2:0]	6M Audio Demodulator AGC control
AGC_6M5 [2:0]	6M5 Audio Demodulator AGC control
CC_VCO [1:0]	VCO current control
CP_5GLO [2:0]	5G VCO buffer current control
CP_FT [2:0]	Charge pump current control (from 50uA to 6mA, default=100uA)
SC_CTL:	CP current test control
MOUT [1:0]	Multi-function output select (RF R divider output, RF prescaler output, lock in detect)
PRES_FT [2:0]	Prescaler tail current control (20 ~ 140uA).

Address 0x03: Synthesizer Register D

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–						SYN_C3 [2:0]			SYN_CZ [2:0]			SYN_RZ [7:0]							
Default	0	0	0	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0

Default: 03980H	
SYN_C3 [2:0]:	Loop filter C3 control
SYN_CZ [2:0]:	Loop filter CZ control
SYN_RZ [7:0]:	Loop filter RZ control

Address 0x04: VCO Switch-Cap Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RFVCO_EX_CAP [4:0]					VCO480_EX_CAP [4:0]					VCO6M _EX_CAP [4:0]					VCO6M5_EX_CAP [4:0]				
Default	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0	0	1	1	1	0

Default: 7ABEFH	
RFVCO_EX_CAP [4:0]:	For RF VCO adjustment
480VCO_EX_CAP [4:0]:	For IF VCOadjustment
6MVCO_EX_CAP [4:0]:	For 6M VCOadjustment
6M5VCO_EX_CAP [4:0]:	For 6M5 VCOadjustment

Address 0x05: DFC Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_RECAL	R [5:0]						OK_RF	OK_IF	OK_6M	OK_6M5	VCODFC_OVP [2:0]			DFC480_OVP [2:0]			AUDFC_OVP [2:0]		
Default	0	1	1	1	1	1	1	0	0	0	0	1	1	1	0	1	0	0	1	0

EN_RECAL:	
R [5:0]:	DFC reference clock control, set default value to 63.
OK_RF:	RF VCO fine tune
OK_IF:	IF VCO fine tune
OK_6M:	6M VCO fine tune
OK_6M5:	6M5 VCO fine tune
VCODFC_OVP [2:0]:	RF VCO setting
DFC480_OVP [2:0]:	IF VCO setting
AUDFC_OVP [2:0]:	6M/6M5 VCO setting

Address 0x06: 6M Audio Demodulator Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	6M_ICP [5:0]						6M_C3 [2:0]			6M_CZ [2:0]			6M_RZ [7:0]							
Default	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0

Default: 82408H	
6M_ICP [5:0]:	6M Charge-Pump current control
6M_C3 [2:0]:	6M Loop Filter Adjusting
6M_CZ [2:0]:	6M Loop Filter Adjusting
6M_RZ [7:0]:	6M Loop Filter Adjusting

Address 0x07: 6M5 Audio Demodulator Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	6M5_ICP [5:0]						6M5_C3 [2:0]			6M5_CZ [2:0]			6M5_RZ [7:0]							
Default	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0

Default: 82408H	
6M5_ICP [5:0]:	6M5 Charge-Pump current control
6M5_C3 [2:0]:	6M5 Loop Filter Adjusting
6M5_CZ [2:0]:	6M5 Loop Filter Adjusting
6M5_RZ [7:0]:	6M5 Loop Filter Adjusting

Address 0x08: Receiver Control Register 1

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–			Reserved			CP_MIXER [2:0]			IFA_GN [2:0]			VAMP_GN [7:0]							
Default	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0

Default: 0FF80H	
CP_MIXER [2:0]:	RF Mixer current control
IFA_GN [2:0]:	IFABF gain control
VAMP_GN [7:0]:	Video Amp gain control 2

Address 0x09: Receiver Control Register 2

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IFAF_GN [2:0]			REGBS_VADJ [2:0]			REGIF_VADJ [2:0]			BC [2:0]			RSSI_SQUELCH_D [7:0]							
Default	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0

Default: B2007H	
IFAF_GN [2:0]:	IFAAF gain control
REGBS_VADJ [2:0]:	BS regulator reference voltage adjust
REGIF_VADJ [2:0]:	IF regulator reference voltage adjust
BC [2:0]:	BC adjust
RSSI_SQUELCH_D [7:0]:	RSSI & noise squelch control

Address 0x0A: Power Down Control Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PD_VCLAMP	PD_VAMP	PD_IF_DEMOD	PD_IFAF	PD_RSSI_SQUELCH	PD_REGBS	PD_REGIF	PD_BC	PD_DIV4	PD_5GVCO	PD_SYN	PD_AU6M	PD_6M	PD_AU6M5	PD_6M5	PD_REG1D8	PD_IFABF	PD_MIXER	PD_DIV80	PD_PLL1D8
5G Default	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	1

Default: **5.8GHz: 10C13H**	
PD_VCLAMP:	Video clamp power down control
PD_VAMP:	Video amp power down control
PD_IF_DEMOD:	IF demodulator power down control
PD_IFAF:	IFAF power down control
PD_RSSI_SQUELCH:	RSSI & noise squelch power down control
PD_REGBS:	BS regulator power down control
PD_REGIF:	IF regulator power down control
PD_BC:	BC power down control
PD_DIV4:	Divide-by-4 power down control
PD_5GVCO:	5G VCO power down control

PD_SYN:	SYN power down control
PD_AU6M:	6M audio modulator power down control
PD_6M:	6M power down control
PD_AU6M5:	6M5 audio modulator power down control
PD_6M5:	6M5 power down control
PD_REG1D8:	1.8V regulator power down control
PD_IFABF:	IFABF power down control
PD_MIXER:	RF Mixer power down control
PD_DIV80:	Divide-by-80 power down control
PD_PLL1D8:	PLL 1.8V regulator power down control

Address 0x0B~0x0E: Reserved

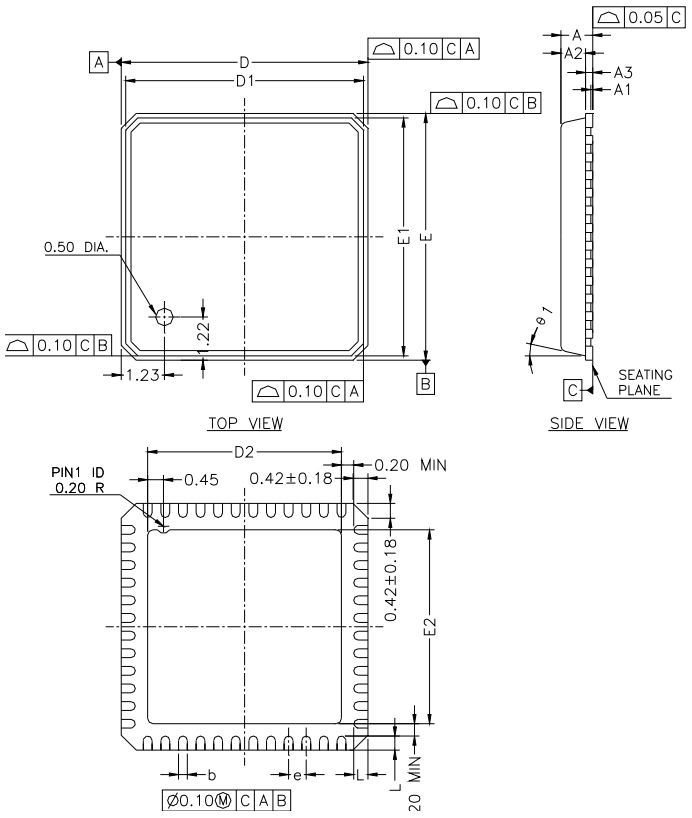
Address 0x0F: State Register

Bits	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–																	STATE [2:0]		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STATE [2:0]	State Name	Description
000	RESET	Reset state.
001	PWRON_CAL	Power on state.
010	STBY	Standby state.
011	VCO_CAL	VCO state.
100~111	Reserved	

PACKAGE

QFN 7X7 48 pins



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.32	0.008	0.010	0.013
D	7.00 bsc			0.276 bsc		
D1	6.75 bsc			0.266 bsc		
D2	5.30	5.50	5.70	0.209	0.217	0.244
E	7.00 bsc			0.276 bsc		
E1	6.75 bsc			0.266 bsc		
E2	5.30	5.50	5.70	0.209	0.217	0.244
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		